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# USB0805C

## Universal Serial Bus Data Line Voltage Suppressor

Designed specifically for protection from ESD across signal lines using the new Universal Serial Bus (USB) protocol. Protects from ESD per the conditions stated in IEC 1000-4-2 and EFT per IEC1000-4-4. Ultra low capacitance minimizes signal attentuation while ultra low leakage current increases battery life for laptops and other portable systems. Applicable for ESD protection on all fast data rate signal lines.

## FEATURES

- Ultra Low Capacitance
- Ultra Low Leakage
- Protects one line pair
- Bidirectional construction
- Standard SO-8 Package

## MAXIMUM RATINGS

- Operating Temperature: -55°C to + 150°C
- Storage Temperature: -55°C to +150°C
- Peak Pulse Power: 300 Watts (8/20 µsec, Figure 2)
- Pulse Repetition Rate: <.01%

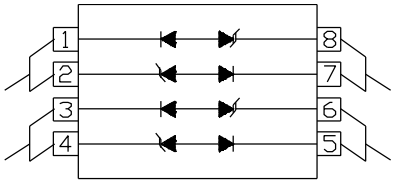
## ELECTRICAL CHARACTERISTICS PER LINE PAIR

### Characteristics @ 25°C Unless otherwise specified

| Part Numbers | Device Marking | Stand-off Voltage $V_{WM}$ Volts | Breakdown Voltage $V_{(BR)}$ @$I_{(BR)}$=1mA Volts | Clamping Voltage $V_C$ @ 1 Amp (Figure 1) Volts | Clamping Voltage $V_C$ @ 5 Amp (Figure 1) Volts | Leakage Current $I_D$ @ $V_{WM}$ mAmps | Leakage Current $I_D$ @ 3.5 V mAmps | Capacitance (f=1 Mhz) @ 3.5 V pF |
|---|---|---|---|---|---|---|---|---|
| | | MAX. | MIN. | MAX. | MAX. | MAX. | TYP. | MAX. |
| **USB0805C** | U5C | 5.0 | 6.0 | 9.8 | 12.5 | 5 | .05 | 5* |

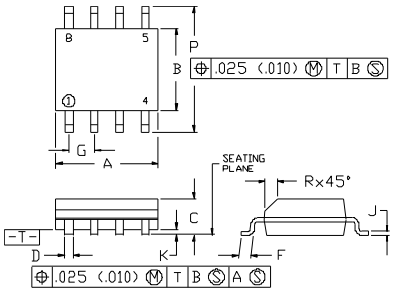
* *Capacitance per protected wire*

### Circuit Diagram




### Mechanical Characteristics

CASE STYLE: SO-8




| | INCHES (MAX/MIN) | MILLIMETERS (MAX/MIN) |
|---|---|---|
| A | .197/.188 | 5.000/4.780 |
| B | .158/.150 | 4.010/3.800 |
| C | .069/.053 | 1.750/1.350 |
| D | .019/.014 | .490/.350 |
| F | .049/.016 | 1.250/.400 |
| G | .050 BSC | 1.27 BSC |
| J | .010/.007 | .250/.180 |
| K | .010/.004 | .250/.100 |
| P | .244/.228 | 6.200/5.790 |

**PULSE WAVE FORM**
(8/20µs)

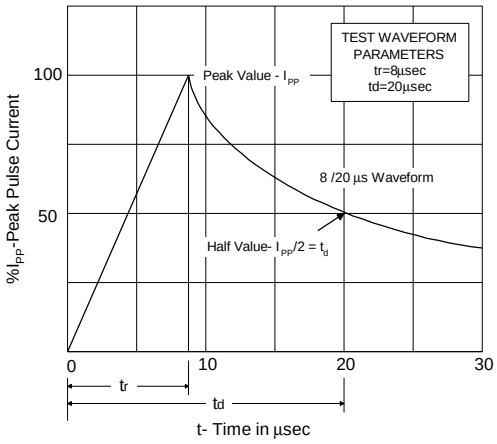



**Figure 1**

**PEAK PULSE POWER vs. PULSE TIME**

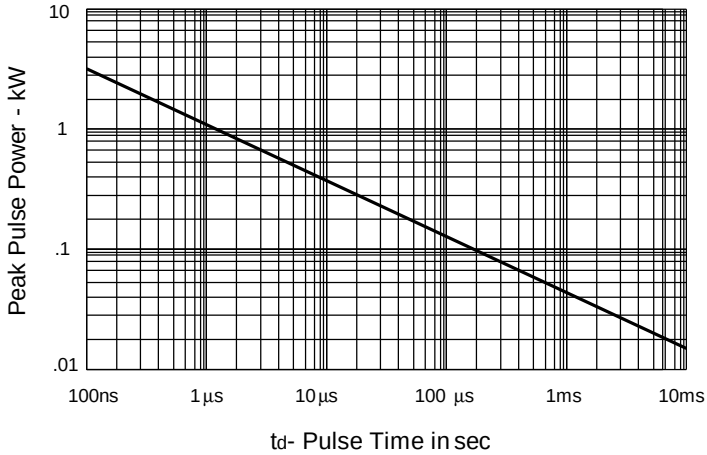



**Figure 2**

DATA SHEET #: MSC0323A
DATE: 09/30/97

# Application Notes for the USB0805C

## Application

USB0805C transient voltage suppressors (TVSs) are designed to protect Universal Serial Bus (USB) I/O ports from damage or latch up caused by ESD. These TVS devices protect two signal lines from each line to ground with typical placement as shown in figure 1. Devices may be used for ESD protection across lines handling data at rates up through 25Mb/s.

## Low Capacitance

The low capacitance of this device presents minimal attenuation to 12 Mb/s high data rate USB signals. This low capacitance is achieved by placing a specialized low capacitance diode in series with the inherently high capacitance 5V TVS chip as shown in figure 2a. A second string in antiparallel, figure 2b, provides bidirectional protection. The net effect is as shown in figure 2c. The combined capacitance of both lines is 5pf max.

Pin interconnections made external to the package link these strings as shown in the circuit diagram (front page) and in figure 3. Pins 1 and 2 are matched to 7 and 8 for one bidirectional line protector and pins 3 and 4 are matched to 5 and 6 for the second bidirectional line protector as illustrated in figure 3.

## Minimizing L(di/dt) Effects

Optimum suppression of fast rise ESD zaps can be realized only by maintaining near zero parasitic lead inductance to minimize L(di/dt) effects. Direct connective paths of the "signal in" and "signal out" traces are virtually noninductive since contact is made at the TVS mounting pad. This provides Kelvin contacts, thus eliminating parasitic inductance effects.

Ground (common) termination pads should tie directly to a ground plane on the board for best results. A long, narrow ground conductor should be avoided since it adds parasitic impedance reducing the protection provided by the TVS.

## Mounting

Locate the USB0805C ESD protector as close as possible to the I/O socket leading to the USB I/O component as illustrated in figure 1 to minimize radiation from the transient as it is directed to ground.

**Figure 3. Opti**

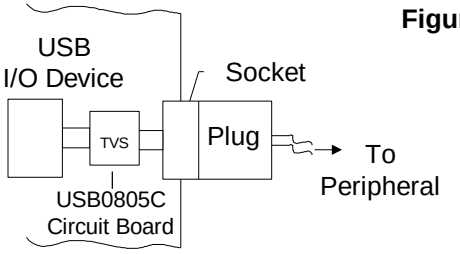



**Figure 1. Typical TVS Placement**

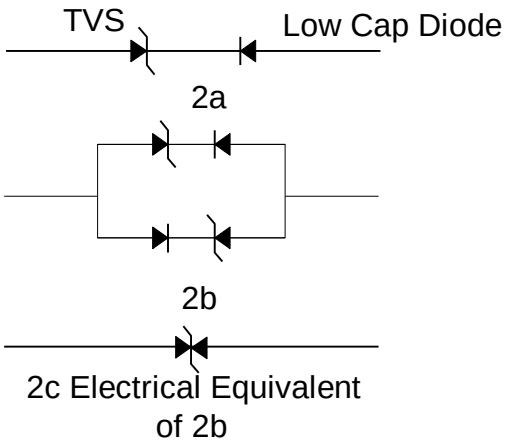



**Figure 2. Low Capacitance**